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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,733	07/24/2003	Tetsuya Nitta	67161-073	8046

7590 12/16/2005

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EXAMINER	
SEFER, AHMED N	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 12/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,733	NITTA ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 16-18* is/are pending in the application.

4a) Of the above claim(s) *1-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13 and 16-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi ("Hayashi") JP 6-318561 (of record) in view of Kanekawa et al. ("Kanekawa") USPN 6,624,474 and Hayashi US PG-Pub 2003/0232490 ("Hayashi '90").

Hayashi discloses in figs. 1-4 a method of manufacturing an integrated semiconductor device having a plurality of semiconductor elements formed in a semiconductor layer and each having a source of a first-conductivity-type semiconductor, a drain 44 of the first-conductivity-type semiconductor and a body region 37/38 of a second-conductivity-type semiconductor between said source and said drain, comprising the steps of: implanting impurities concurrently into at least a predetermined part of the drain of one semiconductor element and into a predetermined part of the drain of another semiconductor element, an implantation mask 2/3 being used that includes a portion corresponding to the drain of said one semiconductor element and having a first opening ratio A as well as a portion corresponding to the drain of said another semiconductor element and having a second opening ratio A' different from said first opening ratio; wherein said one semiconductor element has a breakdown voltage higher than that of said another semiconductor element, and said implantation mask being used has said first opening

ratio smaller than said second opening ratio, and said semiconductor element being adjacent to said another semiconductor element; and annealing said integrated semiconductor device after said step of implanting impurities to diffuse said impurities, but lacks anticipation of a wall shaped element isolation insulating film for isolating said one semiconductor element from said another semiconductor element prior to step of implanting impurities.

Kanekawa discloses in fig. 2 a method of manufacturing an integrated semiconductor device having a plurality of semiconductor elements 2 and 3 formed in a semiconductor layer and each having a source of a first-conductivity-type semiconductor, a drain of the first-conductivity-type semiconductor and a body region of a second-conductivity-type semiconductor between said source and said drain; one semiconductor element being adjacent to said another semiconductor element, and providing, in said semiconductor layer, a wall-shaped element-isolation film 4/101 for isolating said one semiconductor element from said another semiconductor element.

Hayashi '90 discloses (abstract and par. 0031) a wall-shaped element-isolation film (not shown) for isolating one semiconductor element from another semiconductor element; and annealing said integrated semiconductor device after said step of implanting impurities to diffuse impurities.

Therefore, in view of the teachings of Kanekawa's and Hayashi '90, one have ordinary skill in the art at the time the invention was made would be motivated to modify Hayashi's method by incorporating wall-shaped element-isolation film since that would ensure isolation of the semiconductor elements. It would have been obvious to perform annealing said integrated semiconductor device after said step of implanting impurities to

diffuse impurities since that would allow impurities to be accurately introduced into the impurity layer as taught by Hayashi '90.

The combined references, specifically Hayashi '90 (par. 0040) is silent in regard to the recitation calling for "a wall-shaped element-isolation film (not shown) for isolating one semiconductor element from another semiconductor element prior to said step of implanting impurities", however it would have been obvious to form isolation walls prior to step of implanting impurities so as to protect the device elements from each other.

Regarding claim 16, Hayashi discloses in fig. 4 masking portions and openings in the shape of stripes, and said implantation mask is used by being placed with said stripes arranged in the direction parallel to a carrier path from the source to the drain of said semiconductor elements. Similarly, Minato discloses (pars. 0396 and 0404) masking portions and openings in the shape of stripes, and said implantation mask is used by being placed with said stripes arranged in the direction parallel to a carrier path from the source to the drain of said semiconductor elements.

3. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi in view of Kanekawa's and Hayashi '90 as applied to claim 13 above, and further in view of Yoshida JP 6-312918 (of record).

The combined references disclose the method of manufacturing an integrated semiconductor device, but lack anticipation of mesh implantations mask having dot-like openings.

Yoshida discloses in figs. 1-6 the method of manufacturing an integrated semiconductor device including mesh implantation or dot implantation (as in claim 18) mask having dot-like openings being dispersed in a masking portion.

It would have been obvious to obvious to incorporate Yoshida's teachings to enable regions having different concentrations of diffusion to be formed in a single process as taught by Yoshida.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Response to Arguments

4. Applicant's arguments with respect to claims 13 and 16-18 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
December 8, 2005